Filter Bank Analyzer using Programmable IIR Filters

Gaël Nini, Véronique Zimpfer-Jost, Karl Buck

Institut Franco-Allemand de Recherche de Saint-Louis, F-68301 Saint-Louis, France, Email: nini@isl.tm.fr

Abstract

A programmable digital filter based on an enhanced IIR algorithm has been developed at ISL. This filter has a dynamics larger than 60 dB. Its characteristics allow us to use it for the design of a third octave analyzer.

Introduction

The project aims to design a third octave spectrum analyzer for acoustical measurements and to demonstrate the interest of the IIR filter chip developed at ISL for this application.

There are two main types of spectral analyzer architectures: FFT and filter-bank. The filter-bank is more suited to the third octave analysis because it can work with a logarithmic frequency scale.

Digital IIR filter chips are used to realize the filter-bank. The control and the post processing are implemented on a FPGA. The frequency range: 20 Hz - 11 kHz is divided in 3 domains (each one covering 3 octaves), the only difference being the sampling frequency (the coefficients of the digital filters are the same in the 3 domains). To demonstrate the feasibility of the filter-bank, we have developed one board corresponding to the frequency domain 0.178 - 1.4 kHz.

Standardization of third octave filters

The standard used for the filters of the third octave spectrum analyzer is NF EN 61260 [1].

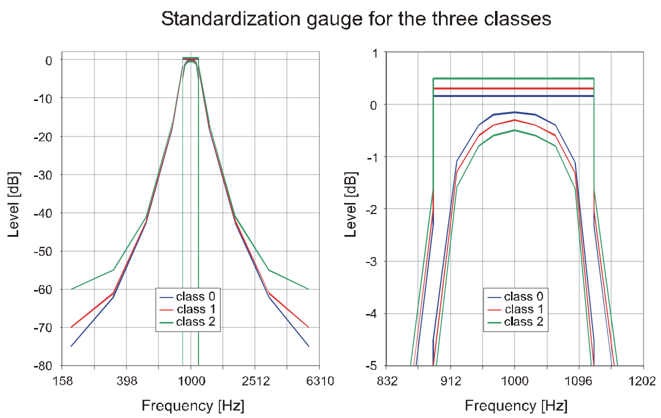

Figure 1: Standard filter response gauge for the three classes for a third octave band pass filter with a center frequency of 1000 Hz (NF EN 61260)

Its specifications are:

- For the center frequencies:

$$f_m = 2^{x/3}.f_r,\ \text{where } f_r = 1000 \text{ and } x \in \mathbb{Z} \quad (1)$$

- For the bandwidth:

$$\left[2^{-1/6}.f_m,\ 2^{1/6}.f_m\right] \quad (2)$$

- For the frequency response: to fit a gauge (Figure 1)

System design

Using digital filtering we can cover the whole frequency range with 3 identical systems, each of them processing 9 third octave bands. The 3 systems correspond respectively to the frequency bands: 22.4 Hz - 178 Hz, 178 Hz - 1.4 kHz and 1.4 kHz - 11.2 kHz.

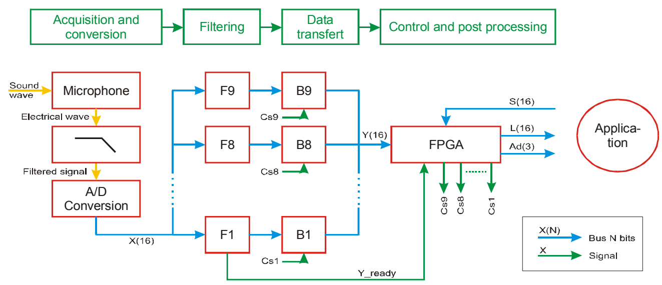

Figure 2: General architecture of the system.

For each system only the sampling rate has to be adjusted. The sampling rates are 1.25 kHz, 10 kHz and 80 kHz.

Each system consists in a Printed Circuit Board, which fulfils 4 functions:

- The analog signal (microphone output) acquisition and the conversion to binary values
- The filtering of the digital signal
- The output to the data bus
- The control, implemented in a FPGA, which allows us to determine the sound level in each band.

Digital filtering with ISL IIR filter chips

The system uses digital filters. The filters implement an IIR algorithm developed at ISL, which improves the dynamics of the low pass filter.

The characteristics of an IIR filter chip are:

- 20 second-order filters can be implemented in cascaded form.
- Programmable with the parallel port of a PC

Moreover, digital filtering allows:

- Enhanced post processing
- Open ended design

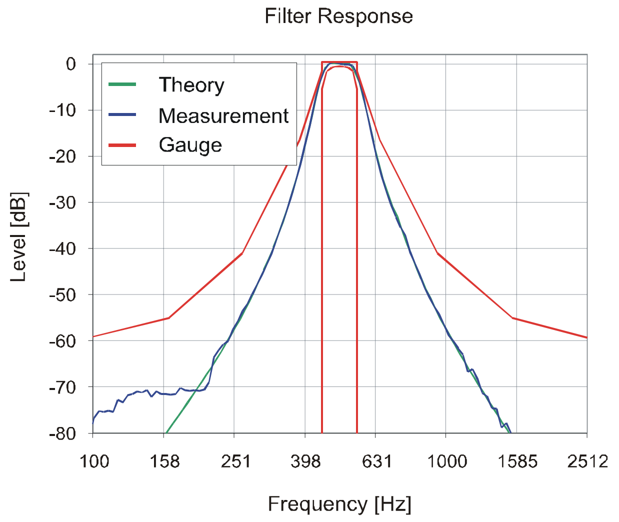

Figure 3: Magnitude of the transfer function for a filter centered to 500 Hz compared to the gauge of class 2.

The 9 filters of the test board have been programmed and tested. The transfer function for the center frequency 500 Hz is represented in figure 3.

Control and post-processing

To implement the controller/post-processor we use a FPGA chip *Xilinx Spartan II*. A VHDL synthesizer allows a high level programming. Each sub-function is designed separately as a "black box". Next, the whole system is assembled by connecting the boxes with the help of a diagram editor.

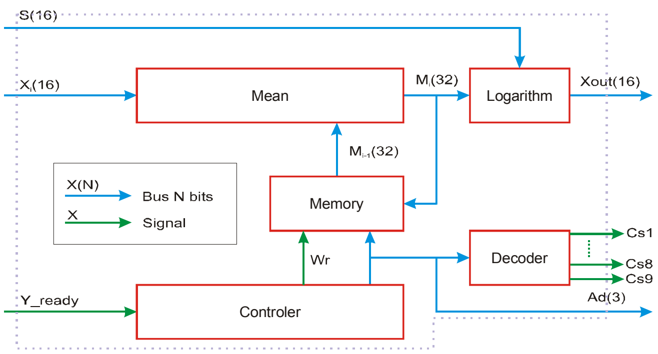

Figure 4: Data flow in the FPGA

The aim of the controller is to enable or disable the output of the buffered data and to authorize the access to the bus only to one filter at a time.

Each filter delivers a 16-bit digital signal. The post processing consists in the calculation of the RMS value and of the Sound Pressure Level in dB_{SPL}.

The recursive averaging algorithm

To calculate the squared mean, we use a converging infinite series:

$$p_{n+1}^2 = \beta p_n^2 + (1-\beta)x_n^2,\ \beta \in [0.9,\ 1] \qquad (3)$$

The square root is obtained by dividing the logarithm by 2.

The logarithm algorithm

Two main steps are necessary to determine the logarithm of a number represented in a fixed-point binary form. First, it is represented in the multiplicative form:

$$X = 2^N \prod_{i=1}^{7} (1+2^{-i})^{x_i}\ ,\ x_i \in \{0,1\} \qquad (4)$$

Next, the factors are turned into the additive form using the logarithm property:

$$\log X = N.\log 2 + \sum_{i=1}^{7} x_i \log(1+2^{-i}) \qquad (5)$$

The logarithm is then calculated using a lookup table.

Conclusion

One board processing 9 third octaves (from 178 Hz to 1.4 kHz) has been realized and tested. The input signal is a pass-band filtered pink noise (flat frequency spectrum when represented in third octave bands).

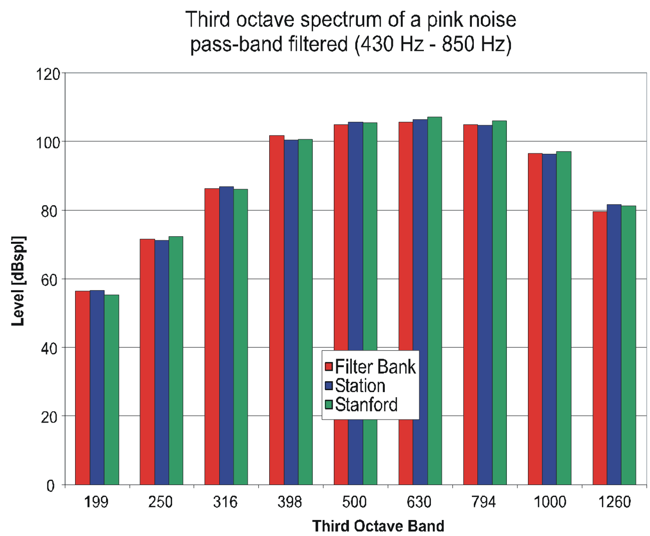

Figure 5: Comparison of the third octaves analyzes obtained with three analyzers

The results are compared with those obtained with two other spectrum analyzers (Figure 5):

- a Stanford, SR780
- a FFT based processor

The results are quite comparable.

References

[1] Grandeurs et unités - partie 7: Acoustique, août 1995. Norme internationale ISO 31-7.